5-GHz and 2.4-GHz Dual-Band RF-Transceiver for WLAN 802.11a/b/g Applications

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***Abstract* — A fully monolithic dual-band radio transceiver chip for 802.11a, 802.11b and 802.11g applications (Table 1) is presented in a 0.25-µm 40GHz BiCMOS technology. The transceiver chip contains a complete receiver chain with low noise amplifier, mixer, programmable gain amplifier, CCK and OFDM channel filters. In the transmit path, a direct-modulation transmitter with integrated anti aliasing filters and programmable gain control is implemented. The frequency synthesizer consists of a fully integrated VCO, a reference oscillator and a phase locked loop for both supported frequency bands of 2.4 GHz and 5 GHz. For a 3 V power supply, the overall power consumptions for 802.11a receive-mode and transmit-mode are 600 mW and 450 mW, respectively.**

I. Introduction

Wireless local area networks have recently emerged in the market and will further propagate rapidly in the communication infrastructure of office and home environments. The 802.11b standard at the 2.4 GHz ISM band provides data rates up to 11 Mbps with the direct sequence spread spectrum (DSSS). This technology first appeared in the market in 1999. The 802.11a standard, released by IEEE in 1999, is based on an orthogonal frequency division multiplexing (OFDM) modulation technology with data rates up to 54 Mbps in the 5 GHz band shown Table 1. The 802.11a standard entered the market with first end-user products in early 2002 [1]. Recently, the IEEE extended the 802.11b standard to higher data rates up to 54 Mb/s by using the OFDM modulation of the 802.11a standard in the 2.4 GHz band, resulting in the new standard 802.11g [2].

This paper presents a fully monolithic dual-band radio transceiver implemented in a 0.25-um 40GHz BiCMOS technology and assembled in a P-VQFN 48 package for small-size, low BOM (bill of material) and high performance WLAN 802.11a, 802.11b and 802.11g solutions.

II. Transceiver Architecture

The transceiver consists of a receiver, transmitter, synthesizer, voltage regulators and 3-wire bus including control logic as shown in Fig.1. A direct conversion architecture for both transmitters (2.4GHz and 5GHz path) was chosen in order to achieve a low-cost solution with a high level of integration compared to an intermediate frequency (IF) based architecture [3]. The receivers for 802.11a and 802.11g are based on a low-IF architecture, which is providing an acceptable impact of dc offsets on the signal to noise ratio (S/N) of the received OFDM signal. As the dc offset requirements are less critical for the 802.11b standard, a direct conversion receiver is used to achieve a low power consumption.

Mode	Data rate/Mbps	Modulation scheme	Freq./MHz	Band
802.11a	6-54	OFDM	5160-5805	UNII
802.11b	1-11	CCK	2412-2484	ISM
802.11g	6-54	OFDM	2412-2484	ISM
802.11g	1-11	CCK	2412-2484	ISM

Table 1. WLAN standards overview

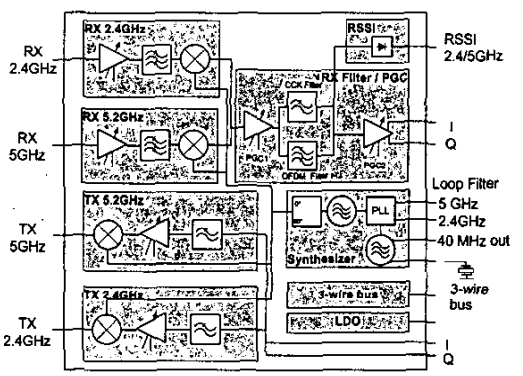

Fig. 1. Block Diagram of the Transceiver

III. Main Block Description

A. Receiver chain

The receive part of the circuit is shown in the upper half of Fig. 1. The whole signal representation is differential.

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The low-noise amplifier (LNA) has differential inputs and requires an external matching network. It can be switched in a high-gain or in a low-gain mode to accommodate a large dynamic range of signals. After an external band-select filter, the signal is down-converted by a complex IQ-mixer, which consists of two Gilbert cell multipliers.

The programmable gain control consists of two programmable gain amplifiers, PGC1 and PGC2. The first reduces the required dynamic range of the channel-select filter, while the second PGC optimizes the signal level after unwanted frequency components are suppressed by the channel-select filter.

To fulfill the requirements of the different modulation schemes, of the various standards, two separate channel-select filters are implemented in order to replace external SAW filters. For the 802.11a and 802.11g OFDM mode a polyphase bandpass filter is used, which is implemented as a Butterworth approximation of 5^{th} order with a center frequency of 10 MHz and a 3dB-bandwidth of 25 MHz. For the 802.11b and 802.11g CCK mode a Chebyshev low-pass filter is used. It has a in-band ripple of about 0.2 dB and a 3 db-cut-off frequency of about 8 MHz. Both filters are implemented with leap-frog structures. The polyphase bandpass filter is in Fig. 2., the low-pass filter is similar, but omitting the resistors that connect the I and Q channel. The measured transfer function of the polyphase filter is shown in Fig. 3. An attenuation of 21 dB and 56dB has been measured at the adjacent channels and alternate channels center frequencies of −10 MHz and −30 MHz, respectively.

An automatic frequency calibration scheme is used for both filters, as well as for the two transmit filters to compensate filter characteristic variations caused by production tolerances.

A received signal strength indicator (RSSI) is required for the automated gain adjustment. It is implemented as a logarithmic amplifier with a cascaded architecture.

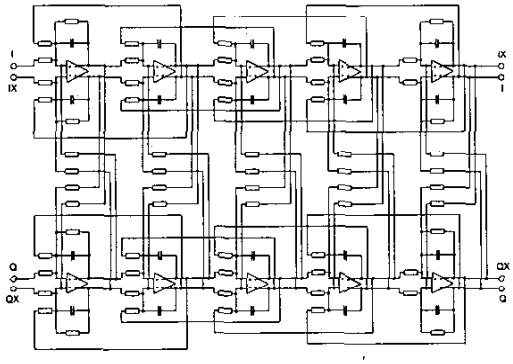

Fig. 2. Channel select filter for the OFDM standards

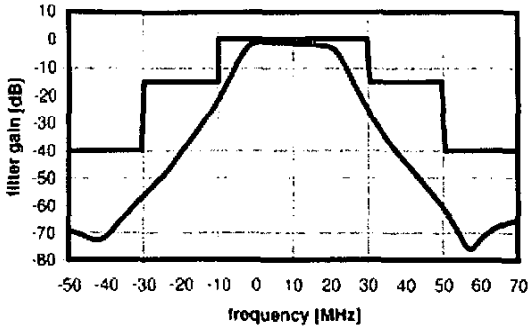

Fig. 3. Measured transfer function of the OFDM polyphase RX-filter in comparison to the filter mask targets.

B. Transmitter chain

The transmitter is a direct modulator that consists of filters at the input, a programmable gain control (PGC) and a quadrature modulator. At the input, anti aliasing filters are required to reduce the harmonic spectra of the digital analog converter. The filters have to be switched to OFDM mode or CCK mode, due to the different channel bandwidth of the two modes.

The quadrature modulator is composed of two identical mixers as shown in Fig. 4. The input stage converts the differential baseband input voltage BBin to currents with the use of an operational amplifier, the transistors M1 and M2 and the resistors R. The gain of the converter is defined by the resistor R that consists of a switching array of binary scaled resistor-cells to compensate the tolerances. With the use of this PGC the output power can be varied. The generated baseband currents are fed to a bipolar switching quadruple by a CMOS current mirror M3, M6 and M4, M5 in each mixer. Bipolar transistors are used for the LO path, due to the higher transit frequencies of the bipolar transistors. Similar structures have been used for the 2.4 GHz and 5.2 GHz band modulators.

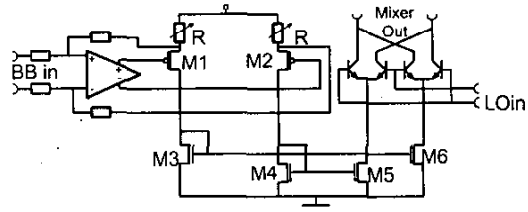

Fig. 4. Transmit mixer circuit

An output power of -9 dBm can be measured at the open collector output of the 5.2 GHz modulator when using an external matching network and an 802.11a compliant OFDM signal. The single sideband suppression of the whole transmit path is 35 dB and the carrier leakage 26 dB

with 1Vpp baseband input. The EVM of the transmit system is measured at -31 dB, which equates to an error vector magnitude of less than 3%. The constellation diagram with a OFDM 64 QAM input signal is shown at Fig. 5. The transmit modulation spectrum compared to the transmit mask specified by the IEEE standard is shown in Fig. 6. The specification requirements are fulfilled with sufficient margins and compare favorably to a recently published heterodyne WLAN solution [3]. The current consumption of the complete transmitter is 155mA.

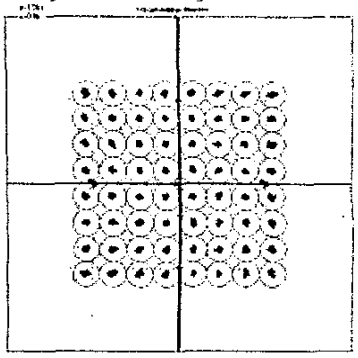

Fig. 5. Transmit constellation measurement

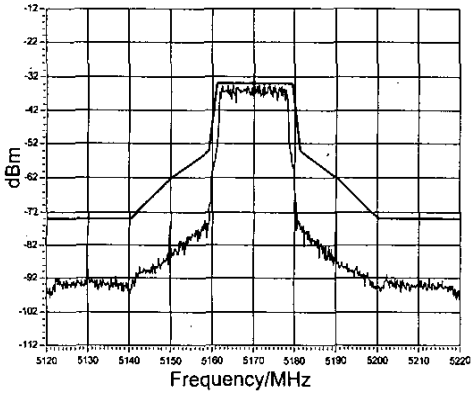

Fig. 6. Transmit spectrum mask

C. Frequency Synthesizer

Different frequency synthesizer circuit blocks are used for the 2.4 GHz and 5 GHz bands to optimize the power consumption. Both synthesizer share one 40 MHz reference quartz oscillator clock, a common reference divider (R) and a programmable RF divider (B/A) (see Fig. 7).

The synthesizer used for the 5 GHz band is realized as an integer-N offset phase-locked loop (PLL) with a voltage controlled oscillator (VCO) at 4/3 of the desired transmitted frequency (see Fig. 7). The quadrature phase carrier is generated by two dividers with divisionratios of 2 and two quadrature mixers [4]. The accuracy of the quadrature phase signal of this architecture is completely independent of the duty cycle of the VCO, which is the main advantage compared to a quadrature phase generation by a divide-by-two circuitry. In addition, this architecture has the advantages of lower VCO and divider frequencies, and higher robustness against crosstalk of harmonics between transmitter and VCO.

A phase deviation of the quadrature phase signals of 1° has been measured, which is a state-of-the-art value for a 5 GHz synthesizer and demonstrates the advantages of the presented architecture.

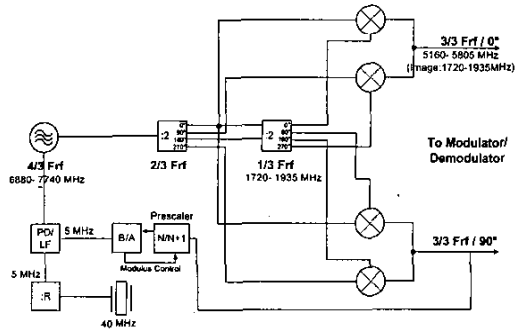

Fig. 7: Block Diagram of 4/3 Offset Synthesizer for 5 GHz band including generation of quadrature signal

The synthesizer for the 2.4 GHz band consists of a VCO and a integer-N PLL using 2 MHz phase detector frequency running both on the double desired frequency. To reduce I-Q phase deviation the generation of the quadrature phase carrier is done in close proximity to the modulator and demodulator.

In order to combine a large tuning range with low tuning sensitivities the VCOs feature a band selection algorithm to set one out of 128 VCO frequency bands followed by an analogue settling process controlled by the PLL [5]. To overcome the wide spread of the tuning sensitivity between highest and lowest selectable VCO band, caused by the different fixed capacitor values seen by the varactor, two VCO cores with different inductors are integrated. Summarizing all tolerances having impact on the frequency accuracy after band selection algorithm performed a fine-tuning sensitivity of 200 MHz/V is sufficient for locking the PLL under all conditions.

For a conventional VCO at 5 GHz [6], a tuning range of 1500 MHz would be required to cover all defined bands over production tolerances. This would result in extremely large tuning sensitivities up to 1500 MHz/V, especially if CMOS varactors with a limited tuning voltage range of 1 V are used. These high tuning sensitivities would have

significant drawbacks with respect to crosstalk, pushing and phase noise, which clearly demonstrates the advantage of the presented VCO architecture.

The normalized 1-Hz phase noise floor of both PLLs is measured to be –215 dBc/Hz, which is comparable to a high performance SiGe-PLL [6]. Thus the rms phase error of the whole synthesizer including quartz oscillator and voltage regulator is measured at the modulator output to be 1° (see Fig. 8) for the 5 GHz band and 0.6° for the 2.4 GHz band.

The 40 MHz reference frequency needed for both synthesizers is generated by a partly integrated Colpitts quartz oscillator, requiring a external xtal and a capacitor. To meet the specification requirement for frequency accuracy of ±20 ppm a digital adjustment array is integrated. The tuning range of this digital programmable oscillator is ±50 ppm enabling the use of xtals with overall tolerance of ±30 ppm and allowing ±20 ppm required tuning range for compensation of circuit tolerances.

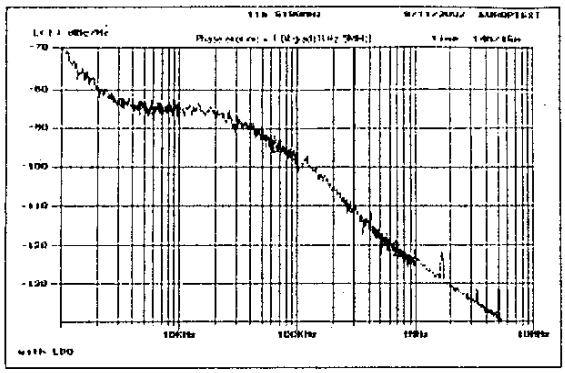

Fig. 8. Synthesizer single sideband phase noise

D. 3-wire bus interface and control logic

The programming of the transceiver is carried out via a 3-wire bus interface. The bus consists of a data signal shifted into the integrated registers on the positive and negative edge of a clock signal and an enable signal storing the shifted data with rising edge into internal latches. Especially for receive PGC settling during OFDM preamble receive a very short programming time below 200 ns is required. This is achieved with a possible clock frequency of 40 MHz and special short 10 bit registers for the PGC gain settings.

Additional 3 digital input pins PON, TXEN and RXEN are available for fast switching receive and transmit modes without any programming sequence.

IV. Conclusion

A 3.0 V WLAN transceiver has been implemented in a 40 GHz BiCMOS Technology. The chip supports the 2.4 GHz and the 5 GHz WLAN standards. A quadrature phase error of 1° has been measured. The transmit error vector is less than 3 % with a 64 QAM input signal. It also fulfills the requirements of the TX-mask and spectrum flatness of the WLAN-standard. The overall power consumption for the 5 GHz modes is 450 mW in transmit mode and 600 mW for receive mode. In the 2.5 GHz CCK modes the power consumption is 340 mW for transmit and 345 mW for the receive mode.

Acknowledgement

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Fig. 9. Chip photograph